REMARKS/ARGUMENTS

Reconsideration of this application in light of the above amendments and following comments is courteously solicited.

The semiconductor device of new independent claim 11 is characterized by the following features:

1. One of first and second semiconductor elements (1, 2) and one of third and fourth semiconductor elements (3, 4) are turned on together, and simultaneously, the other of first and second semiconductor elements (1, 2) and the other of third and fourth semiconductor elements (3, 4) is turned off together; and

2. First and fourth semiconductor elements (1, 4) and said second and third semiconductor elements (2, 3) are alternately switched.

In this arrangement, although heavy current runs through first to fourth semiconductor elements (1 to 4), no local excessive heat can be generated, prohibiting deterioration in electric property of the device, extending service life of the device and improving reliability of the device.

Also, new independent claim 15 is characterized by the following features:

1. A first electrically conductive and radiating layer (11) is mounted between first and second semiconductor elements (1, 2), and a second electrically conductive and radiating layer (12) mounted between third and fourth semiconductor elements (3, 4);

2. An upper electrode of first semiconductor element (1) and a lower electrode of second semiconductor element (2) are electrically connected to each other through first radiating layer (11); and

3. An upper electrode of third semiconductor element (3) and a lower electrode of fourth semiconductor element (4) are electrically connected to each other through second radiating layer (12).

In this arrangement, first and second electrically conductive and radiating layers (11, 12) serve to release outside sufficient amount of heat from first, second, third and fourth semiconductor elements (1, 2, 3, 4) to thereby prevent degradation in electric property of first to fourth semiconductor elements (1 to 4). Also, first and second radiating layers (11, 12) serve to reduce each conductive path for electric current flowing through first and second semiconductor stacks (7, 8) because first and second radiating layers (11, 12) are in direct contact to first and second semiconductor elements (1, 2) and third and fourth semiconductor elements (3, 4).

U.S. Patent No. 6,014,313 discloses three-dimensional multi-chip modules comprising an integrated circuit chips 3, 3', thermal blocks 15, via chips 9 disposed between cooling blocks 19 and top and bottom Si-substrates 7 through inner substrates 1. U.S. Publication No. 2004/0222507 and U.S. Patent No. 5,371,654 only indicate prior art of semiconductor stacks. Accordingly, the present invention as claimed is fully patentable over these references, because none of which disclose or suggest the features and advantages of the present invention as set forth above and claimed in claims 11 and 15. In addition, while Figure 3 of the present application represents a prior art H-shaped bridge circuit, it does not teach a plurality of semiconductor stacks.

An earnest and thorough attempt has been made by the undersigned to resolve the outstanding issues in this case and place same in condition for allowance. If the Examiner has any questions or feels that a telephone or personal interview would be helpful in resolving any outstanding issues which remain in this application after consideration of this amendment, the Examiner is courteously invited to telephone the undersigned and the same would be gratefully appreciated.

It is submitted that the claims as amended herein patentably define over the art relied on by the Examiner and early allowance of same is courteously solicited.

If any fees are required in connection with this case, it is respectfully requested that they be charged to Deposit Account No. 02-0184.

Respectfully submitted,

By /Gregory P. LaPointe #28395/
Gregory P. LaPointe
Attorney for Applicants
Reg. No.: 28,395

Telephone: 203-777-6628
Telefax: 203-865-0297

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